AMENDMENTS TO THE SPECIFICATION:

(1) Please replace paragraph [0017] with the following amended paragraph:

[0017] FIGURE 2 illustrates an exemplary contour plot of the depth of Copper removed during the polishing of a TEOS wafer having a layer of Copper and an underlying Ta barrier layer, using a pad (A32) fabricated using a cross-linked polymer according to the present invention, and a conventional polyurethane pad (IC1400); and

(2) Please replace paragraph [0027] with the following amended paragraph:

[0027] Contour plots of copper surfaces polished using the IC 1400 versus the A32 pad were measured electrically by measuring sheet resistance at 49 points distributed radially across the wafer. Texture maps were generated using software obtained from ResMatÒ Corporation (Resmat map model 487; Montreal, Quebec, Canada). As illustrated in FIGURE 2A, the depth of copper removed across the wafer using the IC 1400 pad ranged from 3000 to 6500 Å, and from 2000 to 5500 Å in a second experiment (not shown). In contrast, as illustrated in FIGURE 2B, the depth of copper removed using the A32 pad was more uniform, ranging from only 4000 to 5250 Å.

(3) Please replace paragraph [0032] with the following amended paragraph:

[0032] As illustrated in FIGURE 3 ~~FIG. 2~~, during the copper polishing stage, the coefficient of friction measured by the tester for the A32 pad was more uniform compared to the IC1000/SUBA IV pad stack. Moreover, during a 300 second polishing period, the IC1000/SUBA IV pad never completely removed the Copper layer, whereas the A32 pad removed the Cu layer in about 220 s,

B3 as determined by an increase the coefficient of friction when the Ta layer was reached ~~(FIGURE 3)~~, or as similarly determined by an decrease in the acoustic signal (not shown).